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At-speed testing made easy

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Today's chip designs are getting smaller and bigger. Feature sizes are moving into nanometer geometries, and gate counts are pushing towards the 100M gate mark. Semiconductor companies creating these nanometer designs are struggling with many issues that result from this shrinking yet increasingly complex design environment. One issue growing in importance is creating high quality, cost-effective tests for these devices.

Companies on the leading-edge of nanometer design discovered the hard way that new types of defects are occurring in these complex nanometer designs. A much higher proportion of the defects are timing related than in previous designs that used older chip manufacturing processes and materials . The defect spectrum now includes more problems such as high impedance shorts, in-line resistance, and crosstalk between signals, which are not always detected with the traditional static-based tests, known as stuck-at tests.

As a result, unless a company adds new types of tests better suited to detect these new failure types, defects per million (DPM) rates increase, which can harm both a company's financial well-being along with their reputation. This problem is forcing companies to re-examine their manufacturing test strategies because traditional test methods are no longer adequate to ensure quality products are shipped to end customers.

Fortunately, the leading-edge companies that first discovered this problem have also identified a solution. Many of these newer defects, like resistive vias and bridges, exhibit defective timing behavior, and therefore, are effectively caught by conducting testing at system speeds. In fact, a leading ASIC vendor documented that their DPM rates were reduced by 30 to 70 percent by adding at-speed testing to their traditional stuck-at tests .

At-speed testing is not new; some companies have been doing it for years. However, most of the at-speed tests created in the past were done with functional test patterns. Unfortunately, these at-speed functional test patterns are very difficult to create since much of the work is done by hand.

Additionally, even if successful patterns can be created, they can be difficult to set up and run on the automatic test equipment (ATE). The actual test coverage these functional patterns provide can be difficult to determine and is usually quite low. An even more difficult problem is diagnosing the source of failure when functional patterns fail.

The industry's leading automatic test pattern generation (ATPG) tools provide fault models that can be used to generate tests targeting at-speed failures. A handful of companies have been using this test technique for many years, working to shape and improve the DFT tools that automate this process. Now the mainstream marketplace, especially those stepping into the realm of nanometer design, is seeing the benefits and moving toward this approach as well.

At-speed fault models

The two at-speed fault models most widely used today include the path delay model and the transition delay model. Compared to static testing with the stuck-at fault model, testing logic at-speed requires a test pattern with two parts. The first part launches a logic transition value along a path, and the second part captures the response at a specified time determined by the system clock speed. If the captured response indicates that the logic involved did not transition as expected during the cycle time, the path fails the test and is considered to contain a defect.

For example, the pattern's launch event may propagate a 0-to-1 (rising edge) transition along a specific path while holding all other conditions constant, as shown in Figure 1. Then the capture event pulses a functional clock to latch in the path's response to the transition. If the "high" value was not detected at the capture point in time, the path fails the test and is considered to have a "slow-to-rise" defect.

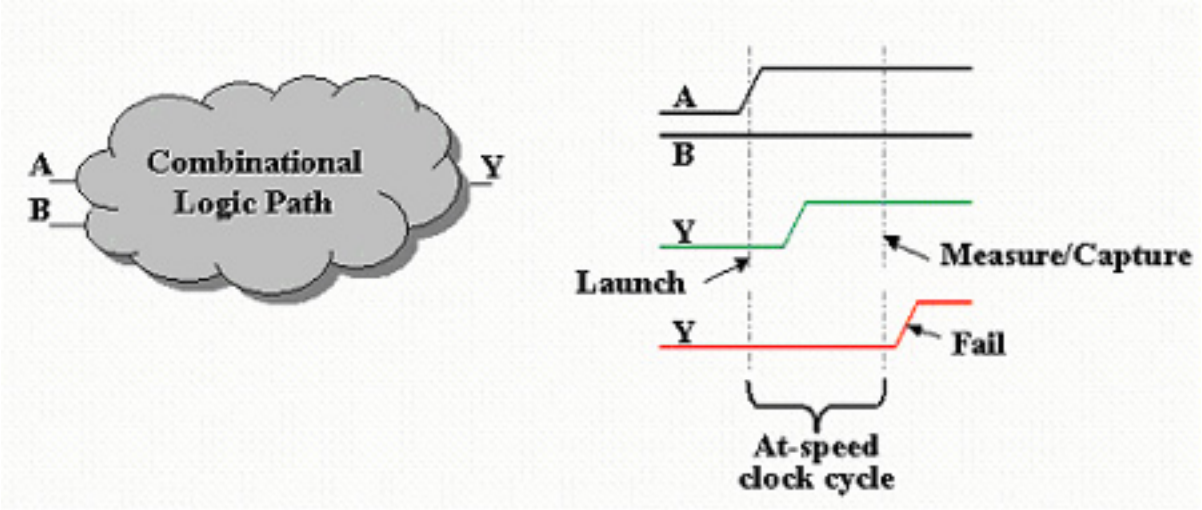

Figure 1 — Pattern launch event propagates transition

Transitions are launched from a path's starting point and captured at the path's end point. The starting point and ending point are typically both scan cells. While paths can start or end at the device input or output pins, testing for these types of paths requires

high resolution clocking typically provided by the ATE. These capabilities are usually only available on high-end testers. Fortunately, some advanced ATPG tools can utilize internal PLLs to automatically provide these high-resolution clocks.

Path delay fault model

Path delay tests target the path delay fault model, which models manufacturing defects or process problems that can cause cumulative delays along the design's critical paths. A static timing analysis tool can identify the design's critical paths, which are used by the ATPG tool to create test patterns for faults along these paths. The total number of possible paths in a design is enormous, so the path delay fault model is generally used for only a limited number of user-defined critical paths. Like the transition fault model, the paths used for path delay testing typically start and end at scan cells.

Path delay patterns are useful for verifying the device's operating frequency and are sometimes used for speed binning. By adjusting the timing of the launch-capture sequence, parts can be tested and rated at various speeds. This technique is useful for products, such as microprocessors, where speed rating is essential.

To implement a path delay test, the process is as follows. A static timing verification/ analysis tool generates a list of critical paths and these paths are used as input to the ATPG tool. When reading in the path file, the ATPG tool checks to make sure each path is real, meaning it is a path that can be exercised during the design's functional mode.

Oftentimes, many of the paths reported by static timing are functional false paths, or in other words, they are paths not actually used in the design's functional operation. This happens because the timing tool is only concerned with adding up the timing delays of the elements in the path. The ATPG tool analyzes the paths and, when it determines that a path is a real functional path, it generates patterns to test it.

When the ATPG fault model is set to path delay, the fault list contains two faults per path, a slow-to-rise and a slow-to-fall fault. It is important to note that when the ATPG tool generates path delay tests and provides a test coverage number, this number reflects coverage of only the loaded paths — not all paths in the design.

Transition delay fault model

Transition tests target the transition fault model, which models manufacturing defects that behave as gross delays on gate terminals (pins). Using the transition fault model, each pin is tested for slow-to-rise or slow-to-fall transition behavior.

For example, a 2-input NAND gate would have six transition faults associated with it. The transition fault model is more widely used than path delay because it tests for at-speed failures at all pins in the design's logic and doesn't require any special user input. While path delay testing only checks for defects on the supplied list of paths, transition testing

automatically chooses small paths in the design that include the targeted fault locations.

Two types of transition tests can be created: launch-off-shift and broadside. In the launch-off-shift approach, the last shift of the scan chain load also serves as the transition launch event. The critical timing is the time from that last shift (or launch) clock to the capture clock, as shown in Figure 2.

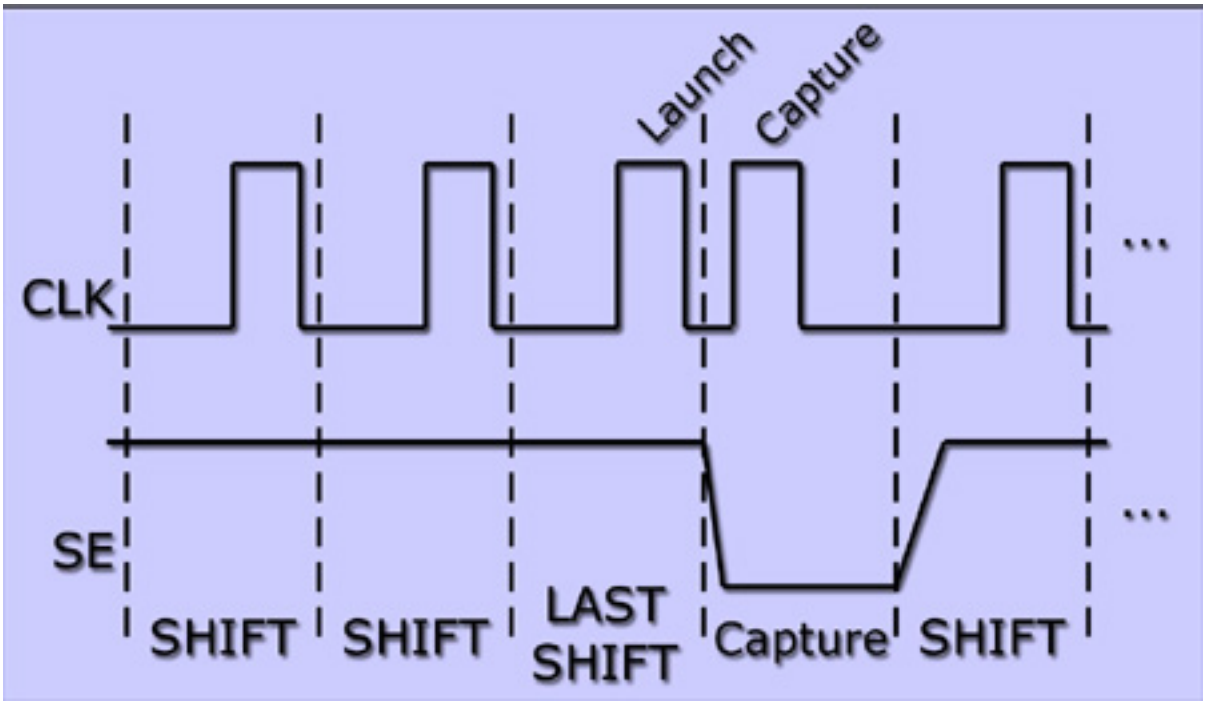

Figure 2 — Launch-off-shift transition test timing

In the launch-off-shift approach, the scan enable signal (SE) must be able to turn off very quickly after the last shift clock and let logic settle before the capture clock occurs. For that reason, the scan enable signal usually needs to be routed as a clock signal to accomplish this. Depending on the design frequency required for the test, the scan chains themselves might also be required to shift at system frequencies.

This can be a limitation because most scan chain shifting is done at lower frequencies. If the chains are shifted and tested at-speed, this could result in an unnecessary yield loss. The main advantage of this launch-off-shift approach is that it only requires the ATPG tool to create combinational patterns, which are quicker and easier to generate.

The other transition testing technique is called broadside. In this technique, the entire scan data shifting can be done at slow speeds in test mode, and then two at-speed clocks are pulsed for launch and capture in functional mode. Once the values are captured, the data can be shifted out slowly in test mode. The timing for this technique is illustrated in Figure 3.

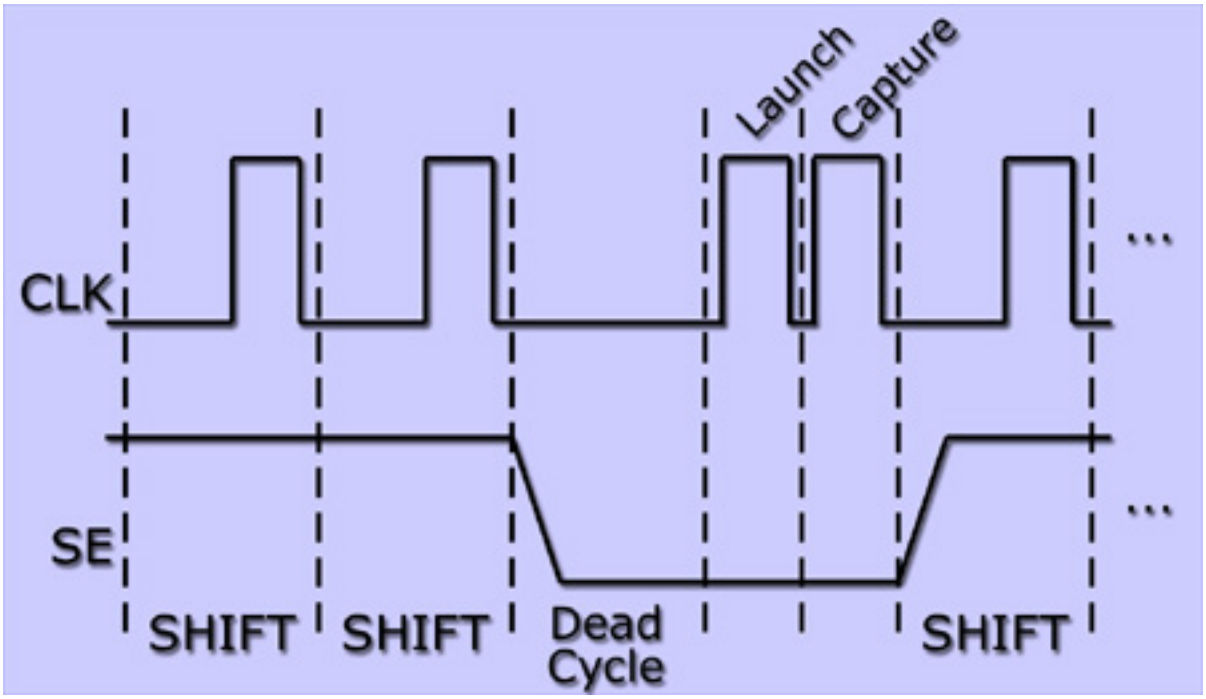

Figure 3 — Broadside transition test timing

The main advantages of this approach are that it does not require scan chains to shift at-speed or the SE signal to perform as a high-speed clock. So, from the design side, it is much simpler to implement.

Additionally, broadside transition testing can also support LSSD-style scan designs. Because of these advantages, most companies have adopted this approach for creating their transition test patterns. The main disadvantage of this broadside approach is that the ATPG problem is now a sequential one, which can increase the test pattern generation time and might result in a higher pattern count.

Some people believe that launch-off-shift patterns provide higher test coverage than broadside testing. This is not necessarily true. The launch-off-shift approach provides additional detection of some non-functional faults that most companies do not want or need to test [2]. Including tests for these faults could even contribute to unnecessary yield loss.

At-speed clocks

An at-speed test clock is required to deliver timing for at-speed tests. There are two main sources for the at-speed test clocks. One is the external ATE and the other is on-chip clocks. Traditionally, ATE has always supplied the test clocks. In some cases, the ATE is still a viable source for the at-speed testing clocks. However, the sophistication and cost of the tester increase as the clocking speeds and accuracy requirements rise.

The second source of clocks can come from inside the chip itself. More and more designs include a phase-locked loop (PLL) or other on-chip clock generating circuitry. Using these functional clocks for test purposes can provide several advantages over using the ATE

clocks. First, test timing is more accurate when the test clocks exactly match the functional clocks. Secondly, the high-speed on-chip clocks reduce the ATE requirements, enabling use of a less sophisticated and, thus, less expensive tester. Figure 4 shows a design with a high-speed on-chip PLL.

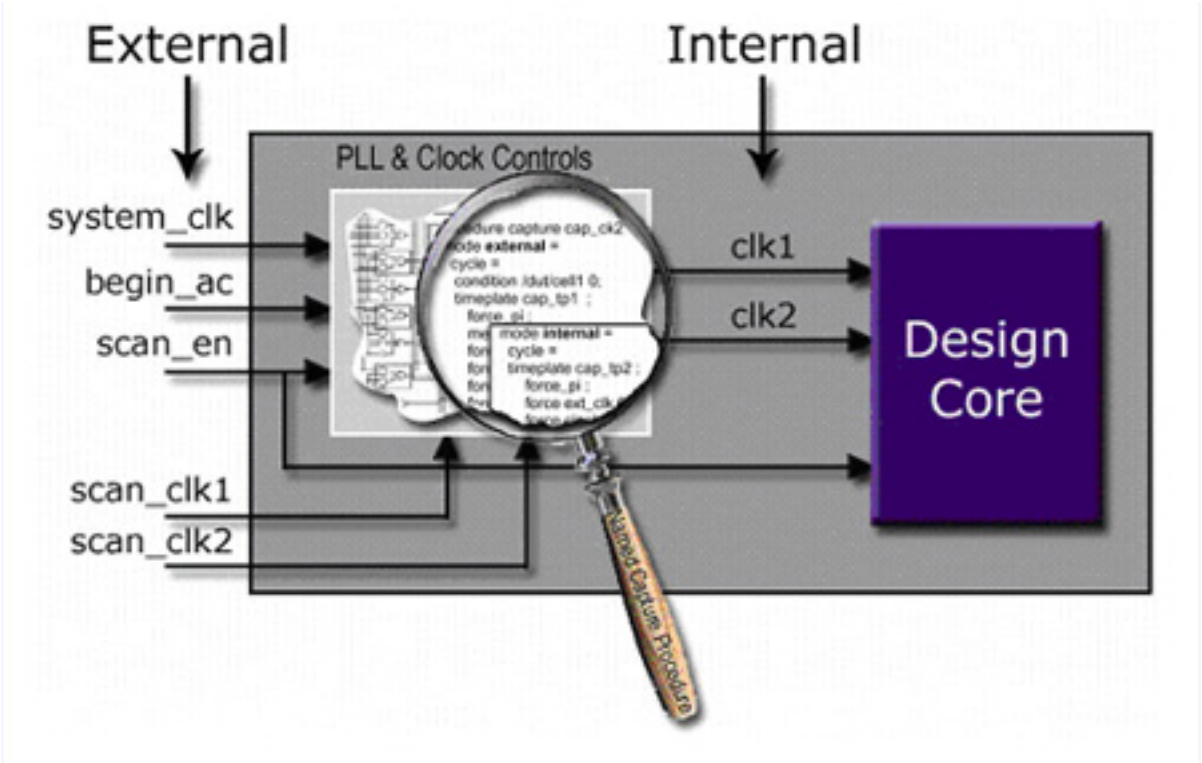

Figure 4 — High-speed, on-chip PLL

In this situation, the design has both internal and external clocks and control signals. By using something called "named capture procedures," the user can specify the functionality and relationships between the internal and external signals. The ATPG tool then uses these relationships to create accurate at-speed test patterns driven by the on-chip clocks.

Control registers are typically used to program which clocks to pulse and when. These internal control registers can be loaded with specific values by the ATPG tool. The ATPG user simply needs to specify the desired register values by using "condition statements" in the named capture procedures. This method is much easier than loading values through a boundary scan test access port (TAP) controller, and it does not require extra external pins to feed in those register values.

Conclusion

At nanometer process technologies, defects are changing, so using only traditional test techniques puts companies at risk of high DPM levels. Ensuring high-quality nanometer designs requires at-speed testing. The industry is quickly adopting an automated at-speed ATPG approach to solve the test quality problem. Current ATPG tools offer functionality to automatically control internal signals for PLL setup to provide accurate

clocking for transition fault testing. Most companies are adding at-speed testing to their production test strategy to achieve the highest quality test cost effectively.

References

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