Exploring the Basics of AC Scan

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This in-depth discussion of scan-based testing explores the benefits, implementation, and possible problems of AC scan.

Today's large, complex chips present an entirely new set of test issues for modern IC design teams. Today, many chip designs run in the multimillion gate range and combine multiple IP cores, some from third-party suppliers. Moreover, the migration from deep-submicron processes with features >100-nm to so-called nanometer processes of <100-nm has brought an entirely new class of speed-related signal-integrity and design-quality issues to the forefront of IC design.

The complexity of large systems on a chip (SOCs) is quickly rendering the development of functional vectors impractical. In many cases, structured test methodologies present a more efficient approach to identifying manufacturing and design defects, characterizing processes, and accelerating binning. AC scan, a key process used in a structured test methodology, can be used to accomplish many of these goals.

Structural Testing

In a structured test approach, engineers use fault models based on validating the structure of the silicon rather than models based on verifying the behavior of the silicon. Structured testing can be performed using the static stuck-at fault model. Gates and wires are proven using design for test (DFT) in the chip with vector generation and the vector grading process automated via EDA tools.

Tests are developed by toggling the suspected defective node to its opposite value, for example, forcing a 1 on a stuck-at 0 node and then applying values at the supporting gate inputs that should allow the good value to propagate to an observation point. If the value at the observation point differs from the expected value, then a fault has been detected.

The vectors used in structural test are highly portable and carry more inherent design information than functional test vectors. More comprehensive vectors allow test engineers to organize tests, develop test programs, and diagnose problems while requiring less familiarity with the chip. In addition, when structured test architectures are

correctly implemented, they can provide more coverage with fewer vectors.

Predominance of Delay
In deep submicron and nanometer designs, it is impossible to describe all faults with a static fault model. A better choice is the dynamically evaluated delay fault model. While very similar to the stuck-at model, it embeds timing characteristics and converts a timing weakness into a Boolean failure: the wrong logic value arrives at the observe point at the sample time.

The gate or transition delay is one delay fault model. It represents itself as a pin value of a gate element that acts as if it has a slow-to-rise (STR) or slow-to-fall (STF) logic transition or as if an interconnect signal has a greater-than-normal propagation delay. A second fault model, the path-delay fault, is similar to the gate-delay fault but resolves the STR and STF concept to the last gate in a path through several gates and net connections.

Various defects that cause errant timing behavior can be modeled as delay faults. These include resistive gate-oxide shorts, insufficient doping that may result in slow transistor switching, incorrect routes such as open and plugged vias, and open or malformed routes that may result in resistive propagation paths (**Figure 1**). Metal bridges or shorted wire connections also can be modeled as delays, but the root cause is the contention with other signals this fault causes.

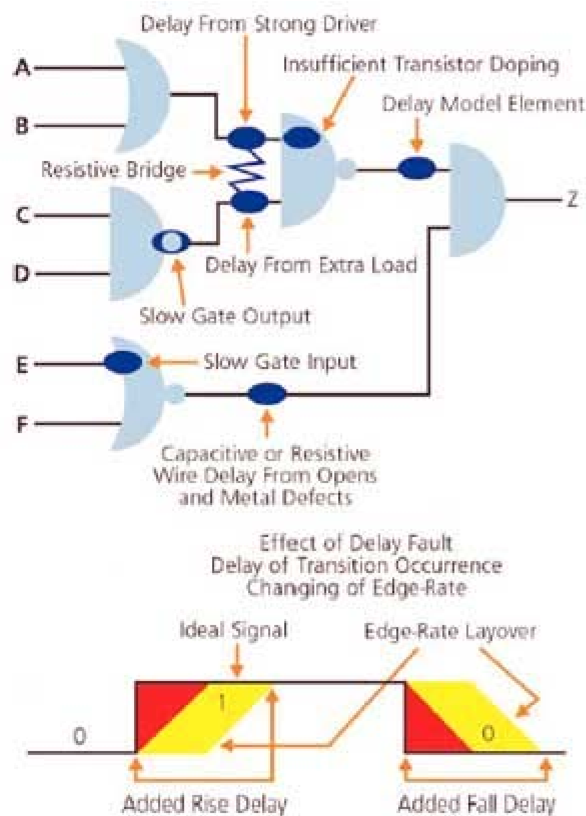

Figure 1. Delay Fault Model

Other defects causing delay-like behaviors to show up in logic are power supply droop, when power rails cannot deliver enough power to drive logic blocks; or clock droop, when a clock-tree driver is of insufficient drive strength or when the clock edge rate is too slow. Some of these effects may be so subtle that they cannot be detected in noncritical paths. Even though small delays may seem like an acceptable defect or fault, they eventually can lead to reliability issues or cause other weaknesses such as excessive leakage.

Diagnosis Dilemma

Many defects in nanometer processes manifest themselves as delays and are located in the wiring, not the gates. Unfortunately, available third-party EDA tools are focused on gate-level analysis. This obviates existing diagnosis processes except for defects that resemble stuck-at faults.

Finding problems in the wiring means analyzing the routes in a diagnostic sense, and this is a very complicated process. It requires the tracing and understanding of a 3-D structure with multiple metal layers, multiple branches, nodes, stems, vertical vias, via plugs, and surrounding complex dielectric materials. As IC designs and the routing strategies have increased in complexity, wires have grown in length and become increasingly convoluted, often surrounded by complex dielectrics to minimize capacitance.

Focus on AC Scan

AC scan conducts an at-speed sample cycle to verify timing compliance. Engineers validate frequency compliance by ensuring that the critical timing paths in a design meet their specification in silicon after manufacturing. This analysis is done on each register or output pin—so-called endpoints.

Pin timing specifications, such as input-setup, input-hold, and output-valid, are verified by ensuring that the one worst-case longest path and the one best-case shortest path, per pin, fall within the specified setup-and-hold timing zone. To locate delay defects, AC scan exercises a number of paths per endpoint, attempting to identify noncritical paths that may incur a delay, which can make them become critical paths.

The term AC scan does not imply testing a part at-speed. In fact, running scan at-speed would require prohibitively high levels of power consumption and force over-design of power rails, clock trees, and the scan architecture. The primary difference between DC stuck-at scan and AC scan is the clocking during the sample cycle. For AC scan, only the launch and capture of a signal need to be at-speed.

AC scan may benefit many high-performance IC designs, but it is

required for embedded complex IP blocks. Also, in today's nanometer-scale processes, delay is the predominant failure mode. Functional vectors are not comprehensive in detecting and isolating structural delay faults. In most cases, the most efficient and comprehensive way to detect these subtle faults is through the use of AC scan with critical paths identified from static timing analysis.

AC scan can replace some functional tests. It can reduce the need for highly precise signal timing and edge placement, complex sequencing capability, and high-frequency data rates. It also offers very portable vectors that are automatically generated by ATPG.

AC Scan Fundamentals

Fault models for AC scan fall into two categories:

• Transition-delay models that detect STR and STF signals and are applied to a gate or route to determine gross delays.

• Path-delay models that detect STR and STF signals over a complete described pathway made of nets, nodes, and gates and mostly are used to detect subtle delays on critical paths.

Faults

A transition-delay test is launched from one state element or primary input, exercises a fault at a gate or node, and is captured at another state element or observed directly at a primary output pin. The primary difference between AC scan and stuck-at scan testing is the addition of timing to the analysis.

The output of the gate is required to be set to the fail value first. A vector pair must be applied to transition the fail value to the passing value and propagate that value to an observation point. If the propagation is slow, then the fail value will be captured.

The diagnostic technique used with transition-delay testing is very similar to that for stuck-at faults. The collection of failing vectors is fault-simulated without fault-dropping, and a single fault common to the collection of failing vectors is identified as the most likely culprit.

Path-delay fault models are used to detect STR or STF nodes in certain propagation pathways, and they are applied to critical paths to identify very subtle delays. Path faults can be viewed as the accumulation of a collection of transition or gate delay faults. The number of paths within a design description is finite but significantly larger than the number of elements and, as a result, difficult to compute. Typically, the path selection process must be constrained in some manner to meet computational limitations.

Debug and diagnostics in path-delay testing are similar to those used in DC scan and transition-delay testing except that diagnostic fault

simulation is not necessary as a first step. The path file used as the fault model to generate the vector becomes the fault dictionary so the first level of diagnostics is implemented by matching multiple path files and looking for common elements.

ATPG

Both the transition-delay and the path-delay models can be analyzed and applied in two time frames to coincide with the need for a vector pair. The first time frame establishes the fail value and launches a transition. The second time frame captures the effect of the transition. The launch-capture analysis is supported by all publicly available ATPG tools and has been for some time. While the vector-generation technology used in AC scan is mature, its application is not.

Clocks

Clocking can be implemented in many ways, but only one at-speed clock pulse is required. For the Mux-D flip-flop type of scan, the scan test clock usually is the system clock. For level-sensitive scan design (LSSD), the scan test clocks generally are dedicated.

For devices that fall within the clocking capabilities of most common testers at speeds under 200 MHz, the clock is connected to the chip package through the system clock pin and used for both the shift and capture clock. At higher frequencies, the system clock often is provided by an embedded on-chip phase-lock loop (PLL) or delay-lock loop (DLL).

In this case, the tester provides a lower speed reference clock. The internal clock applied to the system and often to the scan architecture is the PLL clock. The concern here becomes the power consumption at-speed for both shifting and sampling. Scan toggling can consume more power than the part is rated for. So the problem is to provide a slow shift clock and then allow for an at-speed sample clock.

The most common clocking technique is to select an external scan shift clock or a PLL-generated sample clock via a multiplexer. If switching between clocks becomes a critical timing problem, then the PLL can be modified to chop out pulses so it can effectively be operated at a shift-clock frequency. In this case, at-speed sampling is accomplished when the PLL provides two back-to-back pulses without chopping.

Two Techniques

Assertion and deassertion of the scan shift enable (SE) signal must coincide with the sample clocking. There are two competing methods: launch on shift (LOS) and launch on capture (LOC).

Design of the scan architecture differs for the two methods (**Figure 2**). LOS looks and acts exactly like regular DC scan with only the sample interval changed. It stacks the vector pair in the scan chain so

that a state is installed on the next to last shift (n-1).

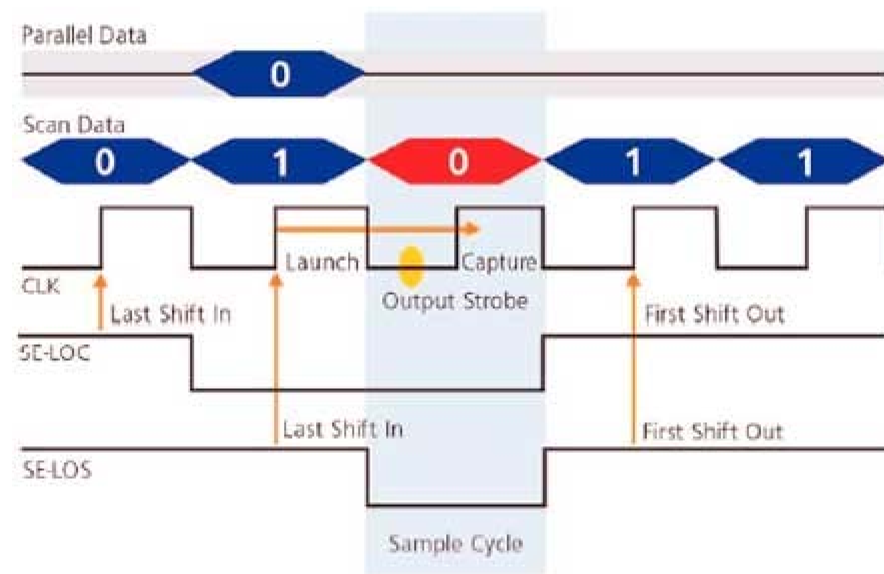

Figure 2. AC Scan Operations

The last shift replicates all of the state data and applies the launch from the launch bit. Then SE is deasserted, and the sample represents the capture. It is easy for the ATPG tool to calculate what to put in the n-1 spaces in the scan chain.

For lower speed designs, the shift and sample clocks are applied at the same frequency, and the entire operation looks like a stuck-at test. For faster designs, shifting is slow, but the at-speed cycle is applied between the last shift and the sample—hence, the term LOS.

When the at-speed cycle has a smaller interval than the shift cycle, the technique is known as cycle-switching or cycle-shrinking. When the at-speed cycle is performed by manipulating the duty cycle so that the last shift has its launch clock late in the period and the capture cycle has its capture clock early in the next period, the technique is known as clock-chopping or duty-cycle modulation.

With LOS, the SE must deassert between the last shift and the now at-speed sample cycle. At high frequencies, this often makes the SE a very critical signal that can no longer be supplied by the tester. The fix is to treat the SE like a clock by making a distribution tree and possibly registering it internal to the chip, which now makes it a problem for the ATPG tool.

The competing LOC method deviates from LOS by conducting two sample cycles instead of one. A state is scanned into the part, then a sample changes the launch bit in its register or LOC, and the next sample captures the at-speed result of the launched transition. Only the LOC cycle is required to be at-speed, and the SE is deasserted in the previous cycle; it no longer is critical.

There are several pros and cons associated with LOS and LOC that impact the software ATPG tool or the hardware scan architecture. LOS is easier on the ATPG tool and results in faster run time and more compressed vectors. However, to generate high coverage, it requires shift-bit independence, which may lead to nonoptimal scan routing, and LOS may generate vectors for invalid test-only or false paths.

LOC needs longer run times from the ATPG tool and results in less vector compression. On the other hand, it does not require any particular bit ordering in the scan chains and allows for more hardware optimizations.

Scan Architectures

Generally, all of the optimizations that apply to DC scan also pertain to AC scan: balancing scan chains, partitioning time domains into scan domains, not supporting load-and-park, and making scan length configurable. Many of the same test rules also are applicable: driven contention is prohibited, clocks cannot be used as data, data cannot be used as clocks, and combinational feedback is not permitted.

The most alarming emerging problem is the effect that nanometer technologies are having on scan architectures. Modern designs suffer from many broken scan chains—blocked scan chains where shift data is stopped or scan chains that exhibit hold-time problems where bit-skipping and data-smearing occur. Unfortunately, advanced fault-tolerant and easy-to-debug scan chain design is not well understood. Nevertheless, common debug methodologies, such as reset and partial reset, and scan chain recovery techniques including mux-around and scan-chain reconfigurability, are being developed.

Conclusion

Despite its many advantages, AC scan is not a mainstream test methodology today. While the technology is mature and proven, its application still is not well understood across the industry. Moreover, the misapplication of the technology in early implementations has resulted in a negative perception of AC scan results.

However, as IC designers move into the nanometer domain, they are confronting a wide array of new yield issues driven by delay defects. Traditional approaches to functional test are too time-consuming and costly to apply to these new multimillion gate IC designs. Using AC scan design, test engineers can shorten the learning curve to improve yield, meet test goals faster and with less effort, and achieve a more deterministic result.

About the Author

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