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UNDERSTANDING AC SCAN-BASED DELAY TESTING

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INTRODUCTION

Economics and time-to-market pressures are forcing chip designers and production test engineers to learn and use structural test techniques such as scan, logic BIST, built-in vector compression, and AC scan. Part of the driving influence is just the sheer size and complexity of the parts and, in many cases, the disaggregated, distributed nature of modern designs with reusable cores, making the use of traditional functional vectors inefficient in creation, sizing, and quality measurement.

The two main reasons for using AC scan are 1) to determine the speed of the part (speed binning); and 2) to identify manufacturing errors and defects (mask problems, process variations or errors, random and systemic defects) that would result in either not achieving the rated frequency or in early reliability failures. Speed binning is discussed in another article in this newsletter, so we will not cover it here. We will discuss the use of AC scan to detect manufacturing defects.

The biggest roadblock to understanding timing and delay defects, however, is not in the implementation and application of AC scan — there are many tools that will insert a scan architecture and many ATPG tools that will automatically create the vectors. The biggest challenge is understanding how and why to use AC scan to meet the established quality goals. Many designers create AC scan vectors correctly, but they misapply them during testing and mistake *coverage* for *quality*.

THE MYTHS OF AC SCAN TESTING

The first myth that must be addressed is that there are significant differences between a DC (or stuck-at) scan architecture and an AC (or delay-testing) scan architecture. This is not true. If you have a DC (stuck-at) scan test architecture, you can perform AC scan testing. The only difference between the two architectures is the clocking.

In a DC scan test architecture, the shift and the sample are generally applied at the same frequency, which is usually between 1MHz and 50MHz. With an AC scan methodology, many organizations have measurement goals and timing requirements anywhere between 1MHz to multi-GHz. Many designers erroneously think they must shift and sample at that speed, and so the scan architecture must be "fully timed" to meet the most aggressive speed of the part. In reality, the vectors can be shifted into the part at any speed, and only the sample cycle (launch-capture vector pair) requires the correct timing interval. This means that only one at-speed clock pulse is needed. *(Note: it has been shown that there are some di/dt issues with shifting too slow and then applying a very high-speed clock, but that will be a topic for a future date.)*

The other problem that confounds designers is the application of launch-on-shift (LOS) versus launch-on-capture (LOC) scan methods (see *Figure 1*). Most people who operate ATPG tools believe that LOS (or launch-on-*last*-shift) results in faster ATPG runtimes, higher coverage for AC-type vectors, and more compressed vectors. The tradeoffs are that 1) the hardware scan architecture must be modified to eliminate shift-bit dependencies (scan-chain bit ordering that restricts the ability to setup a fault or to launch a vector pair); 2) the scan-shift enable (SE) must now be routed as if it were the most critical signal in the part; and 3) the coverage may include false paths. Although it is somewhat true that LOS results in faster runtimes, the key driver of this technique is the mistaken assumption that *higher coverage* is

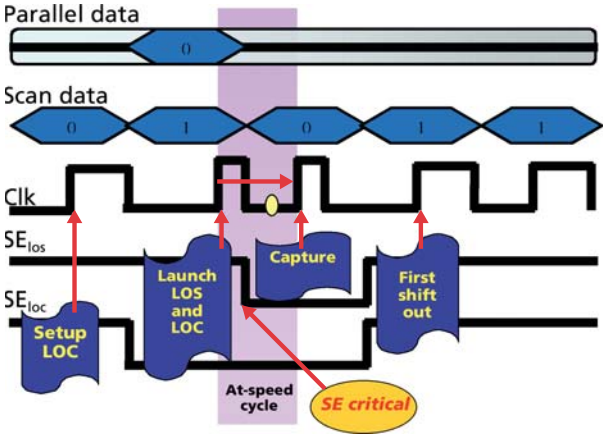


Figure 1: LOC versus LOS scan sequence differences

synonymous with *better quality*. With AC testing, it is the *quality* goal that is not well understood.

With the LOC (two-sample or functional-justification) method, the shift can be accomplished at any speed and the launch-capture vector pair is applied separately, after the SE is transitioned. The SE is in no way critical — there may be an extended time interval or applied dead clocks between shift and the launch-capture application. Similarly, there may be an extended time interval or applied dead clocks after the capture operation and before the first shift out. Since the LOC establishes the initial value of a fault with the scan vector shifted in and then launches the transition using a "functional sample" cycle, the vectors are more likely to be based on real paths than on false paths. The tradeoff here, however, is longer ATPG runtime (more complex analysis as compared to LOS) and less opportunity to pack many fault coverages into one vector (of which the validity will be discussed later).

So, with slow shifting and the LOC method of generating the capture interval, the only difference between a DC scan test architecture and an AC scan test architecture is the clocking. For clocking that is relatively slow (below 200MHz), most automated test equipment (ATE) can provide the necessary clock waveforms; however, for more aggressive clocking, on-chip clock generation logic (DLL, PLL) can be used for the capture pulse.

This means that there are three basic methods for AC scan clocking:

1. The shift and sample clocks source from the ATE (refer to *Figure 2*, configurations A and B). The shift may occur at one speed (slow) and the sample may occur at a different speed (at-speed); or, the tester may apply the same shift and sample speed. This places all of the timing generation requirements on the ATE and only requires that the chip can accept the clocking and represent it through its clock distribution network (the clock pad and tree can handle the applied frequency and edge rate of the clock input).

2. The shift clock may source from the ATE with the sample clock sourcing from the PLL (refer to *Figure 2*, configuration C). This places the timing generation requirements on the embedded PLL and requires a handoff between the ATE and the PLL.

3. The shift clock and the sample clock both source from the PLL (refer to *Figure 2*, configuration D). This places the entire test sequence generation requirement on the PLL. Since operation of the shift architecture at high speeds is a known power problem, and since shift data rates from the ATE are relatively slow, there generally needs to be a pulse chop or frequency reduction applied to the shift portion of the operation.

COVERAGE VERSUS QUALITY

The biggest challenge with AC scan-based testing is understanding what *coverage* means, or what the true goals of testing are. The AC coverage metric is less understood than the differences between stuck-at scan and functional testing. In the latter case, most people know that high stuck-at fault coverage is used to assess manufacturing correctness, and that high stuck-at fault coverage can represent correct functionality if the netlist has been sufficiently verified prior to going to mask; however, if a netlist with a design bug is submitted to ATPG, then the structural vector coverage will prove that the correct "buggy" silicon is produced.

The two main reasons for using AC scan are 1) to determine the speed of the part (speed binning); and 2) to identify manufacturing errors and defects (mask problems, process variations or errors, random and systemic defects) that would result in either no achieving the rated frequency or in early reliability failures.

The other purpose of AC scan testing is for manufacturing correctness. This is where much of the confusion of meeting quality goals occurs. Too many organizations are just trying to achieve high coverage with the transition-delay fault model (erroneously regarding it in a similar vein as stuck-at fault coverage). In many cases, much of the transition-delay coverage is actually no better than stuck-at coverage since the paths being tested are too short compared to the operational (functional) cycle time. For example, if the cycle time is 10ns (100MHz, just to make the math and understanding easier), and if the longest path in a cone of logic only has a 2ns propagation time, then with fixed-cycle testing it would require an 8ns delay fault to observe a failure. This means that any delay defect less than about 7.75ns could hide on this path — and an 8ns delay fault is large enough physically

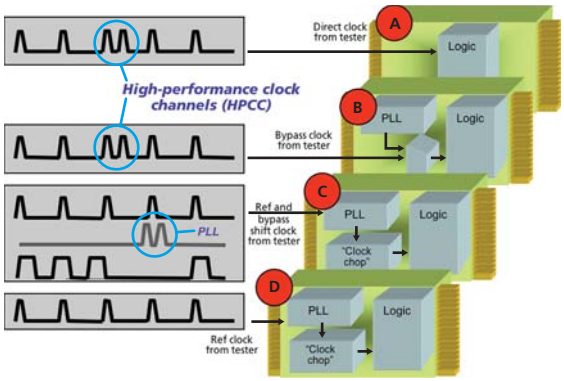


Figure 2: AC scan-based delay testing clock configurations

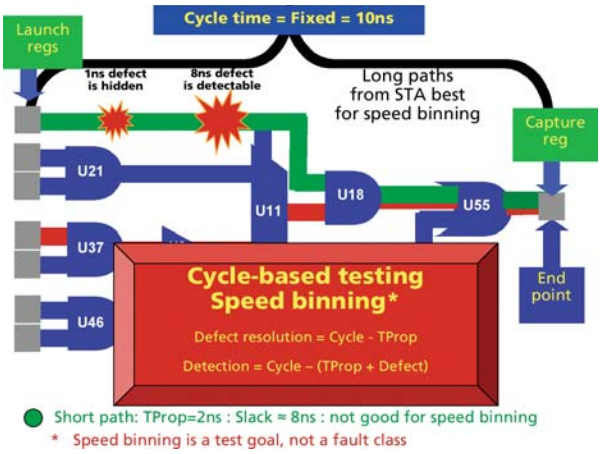


Figure 3: Delay fault coverage versus the real quality metric

and timing-wise that it should be caught by stuck-at vectors (refer to *Figure 3*).

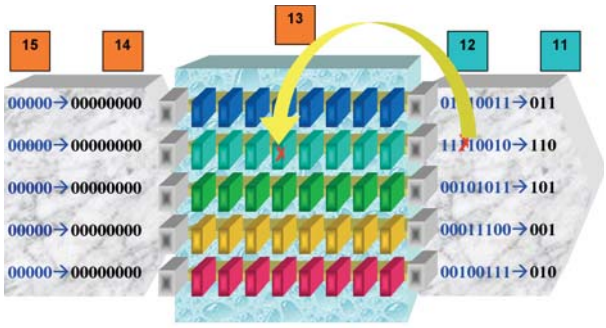
The problem with this example is that using only fixed-cycle testing makes a good portion of the transition-delay coverage unsuitable for screening manufacturing defects. This is where pushing for high transition-delay coverage doesn't make sense, because it does not meet the quality goals of the device. The solution is to use variable cycle testing, or to count only the coverage that falls within some pre-defined margin of timing (size of a defect, percentage of the cycle time, accuracy of the ATE's measurement, and so on).

One of the advantages of structural scan-based testing over functional testing and (with the caveats mentioned earlier) LOC, slow-shift, and at-speed sample is that any given flip-flop can be targeted and tested up to the speed that the clock handling network allows. In many cases, the applied timing is limited by the resolution of the tester or the on-chip clock generation logic. However, any ability to apply tests at a timing less than (frequency greater than) the fixed-cycle timing provides better delay defect resolution. This means that the 2ns flight time within the 10ns cycle time, mentioned in the previous example, could actually be tested near its actual flight time. Making a comprehensive test program requires understanding the timing target of each scan vector and organizing them by sample timing. In this case, the vector compression that is usually applied by ATPG tools — and based on packing as much coverage into a single scan vector as possible — may thwart the quality goal if the coverage is not of similar timing. This is because the slowest endpoint (the one with the longest propagation delay) included within the scan vector will limit the application of the test.

THE ADVANTAGE OF AC SCAN-BASED TESTING

The ability to easily create the AC scan clocking and to easily process variable cycle timing is one of the differentiators between the new generation of DFT (structural) testers and general purpose functional testers. In addition, the ability to capture massive amounts of fail data and to present the test results in the context of design information (in this case, timing targets from STA) and flip-flop location (pattern/chain/bit) leads to rapid debug and diagnosis cycles.

For example, if a scan input pattern, such as pattern 12 in *Figure 4*, is scanned in, then an at-speed sample cycle is conducted by de-asserting SE while applying a clock. Next, scanning in pattern 13 pushes the sample of pattern 12 out of the chip and identifies a failing scan bit within a scan chain by comparing the expected data to the output data. At this point a timing fail may be found. To make sure that the fail is a timing fail, the test should be at a lower frequency — if the pattern passes, then the fail is most likely a timing fail. The failing bit that exits the scan chain is directly related to the scan bit that captured it (if the scan architecture has been verified). In the example, it is bit 5 from the scan output pin on scan chain number



Pattern : Chain : Bit
Patt12: Ch02: Bit05 : TT 2ns
STIL: Scan structures: FlopName
Extra: Delay timing target from STA

Figure 4: Relating flip-flop location to design and fail data

2. This makes the whole address for the failing bit: pattern 12, chain 2, bit 5. In addition, one extra piece of data that is available is that the sample cycle timing on pattern 12 was applied with a 2ns difference between the launch and the capture. Using diagnostic fault simulation, it is possible to identify the potential faults that could cause the timing failure (and there is a high probability that the list of implicated faults can be reduced to just one if the defect or error causes more than one pattern/chain/bit failure).

CONCLUSION

AC scan-based testing is not as difficult or mysterious as it seems if some thought is put into the goals (manufacturing correctness, speed binning, and delay faults) and the method to achieve those goals (fixed-cycle testing and/or variable-cycle testing). The software to generate both the transition-delay and the path-delay vectors has been available for several years and is achieving a good measure of maturity; for both the LOS and LOC methods. And the new generation of DFT or structural testers with built-in scan and AC scan handling and massive data capture capability is making the adoption of AC scan-based delay testing easier and more efficient than ever.

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